CS 631-01 Processor Design Control
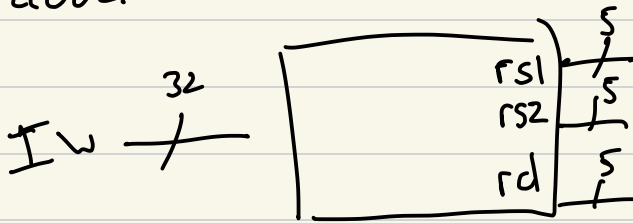
Decoder and Control

Reg Decoder
Imm Decoder
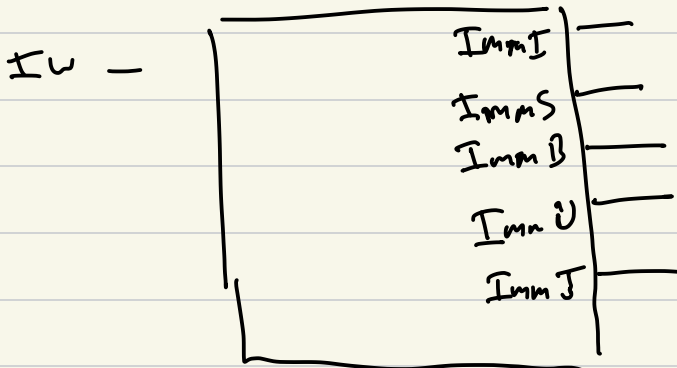Inst Decoder
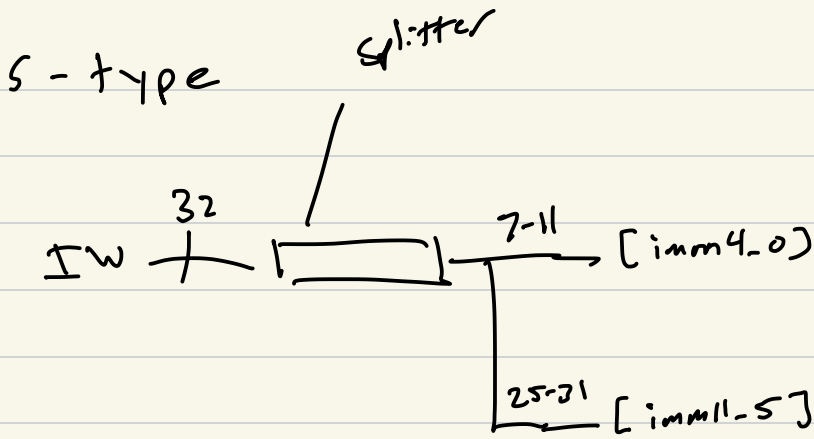
Reg Dacoder

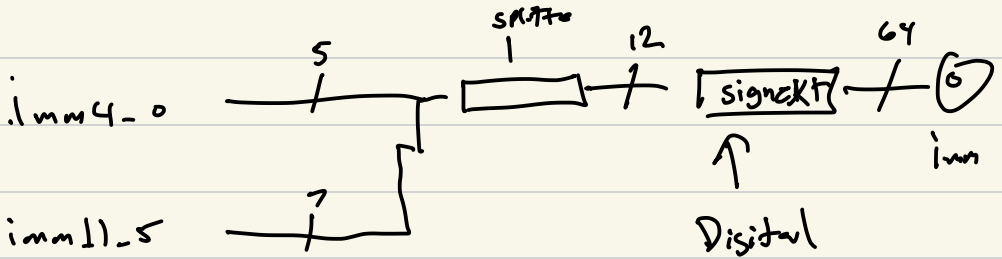Iw —32—→ [box] rs1 —5
rs2 —5
rd —5

one splitter

Imm Decoder

Iw — [box] ImmI
ImmS
Imm B
Imm U
Imm J

S - type

splitter

IW ──┼── 32 ── [   ] ──┼── 7-11 ──→ [imm4-0]
                          │
                          └── 25-31 [imm11-5]

Goal: 64 bit sign extended value

imm4-0 ────┼── 5 ──────┬──── SHIFT── 1 ── [   ] ──┼── 12 ── [sign EXT] ──┼── 64 ──(0)
                       │   ↑   imm
imm11-5 ────┼── 7 ─────┘   Digital

sign ext

──┼── 12 ──●──── [11,11] ────┐   ┌── [   ] ──┼── 64
                             │   │
                             │   ┌─── 57 ───┘
                          12 │   ── ──┼──
                             └── [   ]
                                 [   ]
                                 [   ]
                          63

sign-ext with mux